



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,247	09/24/2003	Perry Lea	200207569-1	3532

22879 7590 06/28/2007
HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER

CHENG, PETER L

ART UNIT	PAPER NUMBER
----------	--------------

2609

MAIL DATE	DELIVERY MODE
-----------	---------------

06/28/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/669,247	Applicant(s) LEA ET AL.	
	Examiner Peter L. Cheng	Art Unit 2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 September 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>9/24/2003</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings are objected to because:
 - **Fig. 3, step 330:** it is assumed that applicant intended to cite “**Imaging Mechanism Ready?**”
 - **Fig. 3, step 345:** it is assumed that applicant intended to cite “**More Pages In Memory?**”
 - **Fig. 4, step 420:** it is assumed that applicant intended to cite “**More Data Pages?**”;

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency.

Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:
 - **Page 5, line 23 - 24** it is assumed that applicant intended to cite "**Maintaining more data pages within the main memory 150 can decrease processing times ...**" instead of "**Maintaining more data pages within the main memory 150 can increase processing times ...**";

If so, appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

Art Unit: 2609

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 – 4, 6 – 12, 14, 16 – 23 are rejected under 35 U.S.C. 102(e) as being anticipated by **Shishizuka [US Patent 6,697,898 B1]**.

As for claim 1, SHISHIZUKA teaches an image forming device comprising:

a scanner configured to scan one or more objects and generate image data representing each of the one or more objects [Fig. 2, scanner 203];

a memory configured to store each of the image data as a page of data [Fig. 108, RAM 203a];

a page frame buffer configured to store a page of data, copied from the memory, that is to be imaged [Fig. 111, Page Memory 511; “Devices used in this copying job are a scanner 510, page memory 511, and printer 512”; col. 73, lines 8 - 10];

an imaging mechanism configured to receive the page of data from the page frame buffer and generate an image from the page of data onto a print media [Fig. 111, Printer 512];

and a dual bus system configured to allow parallel transmission of data where the image data can be transmitted from the scanner to the memory simultaneously with transmitting the page of data from the page frame buffer to the imaging mechanism [The DoEngine is a “single-chip scanning and printing engine”; **col. 6, lines 57 – 58**. It has “two independent buses in its chip, namely an IO bus (B bus) which connects universal IO core and a graphics bus (G bus) which is optimized to transfer ... image data”; **col. 7, lines 21 – 24**. From **Fig. 8**, a “DoEngine” consists of the “CPU 201a, engine interface (engine I/F) 207a, network interface (network I/F) 208a, and external interface (external I/F) 209a”; **col. 70, lines 53 – 55**. Image data from the scanner is stored in “memory 403” (actually, an “SDRAM & ROM Controller”; see **Figs. 4 and 91**). The SDRAM controller interfaces with “RAM 203a” in **Fig. 108**. The “Page Memory 511” in **Fig. 111** is contained within “RAM 203a”].

Regarding claim 2, SHISHIZUKA further teaches the device of claim 1 where

the dual bus system includes a first bus configured to communicate data between the scanner and the memory, and a second bus configured to communicate data between the page frame memory and the imaging mechanism

[A copying job consists of a scanning job and a printing job. “For the scanning job (514), image data for the scanner is controlled by the scanner controller

4302, and written in the memory 403 by way of the G bus 404 and system bus bridge 402. For a printing job, data written in the memory 403 is transmitted by way of the system bridge 402 and B bus 405 to the printer controller 4303 where the data is printed... Data can be output in parallel with input of data"; **col. 73, lines 22 – 34**. Image data from the scanner is stored in "memory 403" (actually, an "SDRAM & ROM Controller"; see **Figs. 4 and 91**). The SDRAM controller interfaces with "RAM 203a" in **Fig. 108**. The "Page Memory 511" in **Fig. 111** is contained within "RAM 203a"].

Regarding claim 3, SHISHIZUKA further teaches the device of claim 2 where

the first bus is configured to allow image data to be loaded into the memory independent of transmitting data from the page frame memory to the imaging mechanism [As previously noted in claim 2, "Data can be output in parallel with input of data"; col. 73, lines 22 – 34].

Regarding claim 4, SHISHIZUKA further teaches the device of claim 2 further comprising:

a first processor configured to control communication of the image data to the memory [Fig. 4, scanner controller 4302];

and a second processor configured to control communication of the page of data from the page frame memory to the imaging mechanism [Fig. 4, printer controller 4303].

Regarding claim 6, SHISHIZUKA further teaches the device of claim 4 where

the first and second processors include application specific integrated circuits [Both first (i.e., scanner controller) and second (i.e., printer controller) processors are contained in the "DoEngine" application-specific IC (ASIC). "The DoEngine is a large-scale ASIC"; col. 63, line 35].

Regarding claim 7, SHISHIZUKA further teaches the device of claim 1 where

the page frame buffer is configured to store one or more pages of data as one or more units [Fig. 111, Page Memory 511; "Devices used in this copying job are a scanner 510, page memory 511, and printer 512"; col. 73, lines 8 - 10].

Regarding claim 8, SHISHIZUKA further teaches the device of claim 1 where

the dual bus system is configured to communicate data by direct memory access ["The GBI_SCC performs the DMA transfer of acquired image data to the memory controller (MC) 403. The image data transferred by DMA is written by the MC 403 into the SDRAM"; col. 66, lines 46 – 50. "By the DMA transfer of the GBI_PRC, the printer controller (PRC) inputs the image data written in the SDRAM sequentially into the internal FIFO"; col. 66, lines 59 - 61].

Regarding claims 9, SHISHIZUKA teaches the device of claim 1 further including

a storage device configured to store image data from the scanner once the memory is full [Fig. 108, external storage device 204a].

Regarding claim 10, SHISHIZUKA further teaches the device of claim 1 where

the page of data includes at least three planes of color data [Fig. 44, video RGB (red, green, blue) image data from the "scanner device I/F" 4401].

Regarding claim 11, SHISHIZUKA teaches a method of processing image data in an image forming device, the method comprising:

scanning one or more sheets of print media and generating one or more image data pages [with a scanner, Fig. 2, 203];

loading the one or more image data pages into a memory [Fig. 108, RAM 203a];

copying a first image data page into a page frame memory from the memory to prepare for imaging [Fig. 111, Page Memory 511];

and transmitting the first image data page for imaging to an imaging mechanism [Fig. 111, Printer 512]

where the transmitting can occur in parallel with the loading [As previously noted for claim 2, "Data can be output in parallel with input of data"; **col. 73, lines 22 – 34**. Image data from the scanner is stored in "memory 403" (actually, an "SDRAM & ROM Controller"; see **Figs. 4 and 91**). The SDRAM controller interfaces with "RAM 203a" in **Fig. 108**. The "Page Memory 511" in **Fig. 111** is contained within "RAM 203a"].

Regarding claim 12, SHISHIZUKA further teaches the method of claim 11 further including

converting the first image data page into print ready data before transmitting for imaging [As shown in **Fig. 68**, printer video clock unit **6602** converts 64-bit image data to 24-bit RGB image data].

Regarding claim 14, SHISHIZUKA further teaches the method of claim 11 further including

loading one or more image data pages into a mass storage device once the memory is full [Fig. 108, external storage device **204a**].

Regarding claim 16, SHISHIZUKA further teaches the method of claim 11 further including

sequentially copying the one or more image data pages from the memory to the page frame memory to prepare for imaging [“By the DMA transfer of the GBI_PRC, the printer controller (PRC) inputs the image data written in the SDRAM sequentially into the internal FIFO”; col. 66, lines 59 - 61].

Regarding claim 17, SHISHIZUKA teaches a system for formatting image data for an image forming device, the system comprising:

a first data bus [Fig. 4, G Bus 404];

a first memory configured to store image data pages, the first memory being configured to receive the image data pages over the first data bus [Fig. 4, SDRAM & ROM Controller 403; Fig. 108, RAM 203a];

a second memory configured to load a page of data that is to be imaged, the page of data being received from the first memory [Fig. 111, Page Memory 511];

and a second data bus configured to communicate the page of data from the second memory to an imaging mechanism where the page of data can be transmitted to the imaging mechanism in parallel with the first memory receiving the image data pages [Fig. 4, B Bus 405].

Art Unit: 2609

Regarding claim 18, SHISHIZUKA further teaches the system as set forth in claim 17 further including

an imaging processor configured to process the page of data from the second memory into print ready data that can be processed by the imaging mechanism [As shown in Fig. 68, printer video clock unit 6602 converts 64-bit image data to 24-bit RGB image data].

Regarding claim 19, SHISHIZUKA further teaches the system as set forth in claim 18 where

the imaging processor includes one or more logic circuits each configured to process one plane of color data from the page of data [As shown in Fig. 68, printer video clock unit 6602 converts 64-bit image data to 24-bit RGB image data].

Regarding claim 20, SHISHIZUKA further teaches the system as set forth in claim 17 where

the first data bus is in data communication with a scanning device configured to scan objects and generate a image data page including color data representing each scanned object [Fig. 2, scanner 203].

Regarding claim 21, SHISHIZUKA further teaches the system as set forth in claim 17 further including

a storage disk device configured to store overflow image data pages after the first memory is at capacity [Fig. 108, external storage device 204a].

Regarding claim 22, SHISHIZUKA further teaches the system as set forth in claim 17 where

the system is configured to copy an image data page from the first memory to the second memory by direct memory access [“The GBI_SCC performs the DMA transfer of acquired image data to the memory controller (MC) 403. The image data transferred by DMA is written by the MC 403 into the SDRAM”; col. 66, lines 46 – 50. “By the DMA transfer of the GBI_PRC, the printer controller (PRC) inputs the image data written in the SDRAM sequentially into the internal FIFO”; col. 66, lines 59 - 61].

Regarding claim 23, SHISHIZUKA further teaches the system as set forth in claim 17 where

the system is configured to process image data pages as one or more data units [Fig. 111, Page Memory 511; “Devices used in this copying job are a scanner 510, page memory 511, and printer 512”; col. 73, lines 8 - 10].

Art Unit: 2609

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 5, 13, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shishizuka [US Patent 6,697,898 B1].

Regarding claim 5, SHISHIZUKA does not specifically teach the device of claim 4 where
**the second processor is configured to decompress the page of data and
transmit pulse modulated wave patterns to the imaging mechanism based
on the decompressed page of data**

However, Shishizuka does teach that the "DoEngine can be combined with a rendering engine having a PCI bus interface and a compression/elongation engine"; **col. 7, lines 18 – 20**. It would have been obvious to one of ordinary skill in the art at the time the

Art Unit: 2609

invention was made to add a compression/de-compression engine in order to efficiently use available RAM and external storage (e.g. a hard disk).

Regarding claim 13, SHISHIZUKA does not specifically teach the method of claim 11 further including

holding the first image data page in the page frame memory until the imaging mechanism is ready to print.

However, Shishizuka does teach that the print controller control register 6604 includes a "printer device status register"; col. 44, line 45. It would have been obvious to one of ordinary skill in the art at the time the invention was made to check the printer device status register and confirm that the printer was in a state to receive data. For example, if the printer were in an error state (e.g. a paper jam), image data would be held in the page frame memory until the error condition cleared.

Regarding claim 15, SHISHIZUKA does not specifically teach the method of claim 11 further including

removing an image data page from the memory after the image data page has been imaged and outputted from the image forming device.

Art Unit: 2609

However, It would have been obvious to one of ordinary skill in the art at the time the invention was made to either remove or overwrite the image data from memory in order to re-use the memory for subsequent pages.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- U.S. Patent 5,864,652
- U.S. Patent 6,222,636
- U.S. Patent 6,226,102

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peter L. Cheng whose telephone number is 571-270-3007. The examiner can normally be reached on MONDAY - FRIDAY, 8:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Kelley can be reached on 571-272-7331. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2609

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

plc


CHRIS KELLEY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2000